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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,151	07/15/2003	Matthew A. Kliesner	72206	8500

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
01/10/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

creganoa@addmg.com

Office Action Summary	Application No.	Applicant(s)	
	10/620,151	KLIESNER ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The RCE filed on 12/17/2007 has been entered. Claims 1-15 are still pending in this Office action.

Response to Arguments

2. Applicant's arguments filed on 12/17/2007 have been fully considered but they are not persuasive. ***See Full Explanation in the following claim rejection***.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vergnes et al. U.S. Patent 5,977,805 in view of Perrot U.S. Patent 6,988,227 B1 and John L. Stensby, "Phase-Locked Loops: Theory and Applications", 1997, ISBN 0-8493-9471-6.

Regarding claim 1, Vergnes et al. teaches in FIG. 6 a circuit diagram of a phase lock loop employing the frequency synthesis circuit of FIG. 1 as a numerically controlled oscillator.

In column 6 line 40 via column 7 line 45, with reference to FIG. 6, an input signal containing the digital tuning word is applied to the phase lock loop along line 81. The input signal is a base band signal, which includes the phase of the system transmitter clock itself at a nominal frequency, where the phase of the clock signal is used as a reference for a local oscillator in the receiver at the nominal frequency.

Phase comparator 85 transmits recovered input data to filter 87 for elimination of spurious signals and then transmitted to oscillator 89, which is a numerically controlled oscillator illustrated in FIG. 1. FIG. 1 discloses a multi-tap delays line 4. The numerically controlled oscillator 89 selects from available phase delays (shown in FIG. 1) to provide a recovered clock signal along line 93. This output frequency is integrated, in order to generate the phase, by a second integrator 95 in a feedback loop 97 and transmitted back to phase comparator 85 which provides a phase lock. The available phase delays of oscillator 89 resemble the delays available in the delay line 41 of FIG. 1. The PLL in FIG. 6 further discloses an error filter 87 and accumulator 17 (shown in FIG. 1 respectively).

Vergnes et al. differs from the pending claim in that Vergnes does not disclose a gain element as claimed in the application claim.

Perrot discloses a conventional PLL 100 (shown in FIG. 1) being used to perform a clock recovery operation. The conventional PLL includes conventional phase detector 102, loop amplifier and filter 112 and VCO 108.

Vergnes et al. and Perrot teachings teach in the same field of endeavor. Because loop amplifier would further enhance the phase error to speed up the pull in time,

therefore, one of ordinary skill in the art at the time the invention was made would have been motivated to modify Vergnes et al. PLL to further include a loop amplifier.

In response to Applicants' arguments on page 11 in the Remarks that the Examiner has not shown that Vergnes et al. is a second order phase locked loop and that it inherently includes closed loop gain. The Examiner's statement on its face does not specify the amount of gain whether it is positive, negative or fractional in nature.

The Examiner further introduces the textbook "Phase-Locked Loops: Theory and Applications" written by John L. Stensby. On pages 22-23, John L. Stensby teaches, in FIG. 2.5, modeling of a linear PLL including a loop filter F(s). Equation 2.3-4 discloses a closed loop transfer function H(s) including a closed loop gain constant G. As further shown on page 76, by definition, a second order PLL includes the loop filter, equation 3.2-1. Since the PLL in FIG. 6 as taught by Vergnes et al. includes loop filter 87, the PLL is a second order PLL, by definition. Furthermore, the closed loop transfer function H(s) including a closed loop gain constant G.

In response to Applicants' arguments on page 11 in the Remarks that the Examiner's statement on its face does not specify the amount of gain whether it is positive, negative or fractional in nature. In certain general phase locked loops, positive gain would result in oscillation and not stability. The Examiner has not shown that the application of gain in the Vergnes et al. reference would result in an operative system. The same question applies to the second assertion of official notice. A positive gain, in excess of unity, may well result in instability.

The Examiner's position is that the stability issue in designing a stable PLL is well known in the art. As explained by John L. Stensby on page 23, stability of the linear PLL model requires that the poles of the closed loop transfer function must be in the left half of the complex plane; see further FIG. 3.1 showing root locus for a second-order PLL. In designing the PLL as shown in FIG. 6, Vergnes et al. would have known the stability issues. As further explained on pages 134-135, a pull-in is a process in which the PLL achieves phase lock naturally and without assistance. The pull-in time is a function of the PLL initial condition, and it is defined as the time required for the PLL to go from this initial condition to a frequency-locked state. John L. Stensby further teaches that all practical PLL have an upper limit on their pull-in range. The pull-in phenomenon is unreliable and slow in many applications. John L. Stensby further suggests additional circuits that aid the acquisition process.

In view of the aforementioned teachings, there is no question to an average skill in the art that a loop amplifier would further enhance the phase error signal and speed up the acquisition process.

Vergnes et al. differs from the pending claim in that Vergnes does not disclose a gain element as claimed in the application claim.

Perrot discloses a conventional PLL 100 (shown in FIG. 1) being used to perform a clock recovery operation. The conventional PLL includes conventional phase detector 102, loop amplifier and filter 112 and VCO 108.

Vergnes et al. and Perrot teachings teach in the same field of endeavor. Because loop amplifier would further enhance the phase error and speed up the acquisition

process, therefore, one of ordinary skill in the art at the time the invention was made would have been motivated to modify Vergnes et al. PLL to further include a loop amplifier as disclosed in a conventional PLL.

Regarding claims 2, in column 7 lines 15-45, Vergnes et al. further discloses that the phase comparator 85 compares the phase relationship between the recovered clock signal and an input data signal to generate a difference signal fed to oscillator 89, which is a numerically controlled oscillator as illustrated in FIG. 1. The frequency of the recovered clock signal over time may be higher or lower in frequency than the frequency of the reference clock on line 91. In view of the foregoing disclosure, in response to the difference signal, an output of the delay line provides later-in-time delay relative to the previous output of the delay line when the frequency of recovered clock signal is lower than the frequency of the reference clock; see also column 7 lines 1-45.

Regarding claim 3, the rejection argument is very similar to claim 2 rejection. In this case, in response to the difference signal, an output of the delay line provides earlier-in-time delay relative to the previous output of the delay line when the frequency of recovered clock signal is higher than the frequency of the reference clock.

Regarding claim 4, claim is rejected on the same ground as for claim 2 because of similar scope.

Regarding claim 5, in column 1 line 55 via column 2 line 50, Vergnes et al. teaches the input digital word is fed to an accumulator whose value reaches periodically a threshold. This period depends on the input digital word value, which depends on the phase difference at the output of phase comparator 83 shown in FIG. 6. The accumulator 17, of course, overflows. In Vergnes et al. teachings, accumulator underflow and overflow are both called "overflow". The total amount of delay is fed to a multiplexer which operates on an incoming digital word by shifting the local oscillator frequency signal by a phase delay unit each time a new increment occurs on the integrator 13 (counter) located just before the multiplexer 33 shown in FIG. 1.

Regarding claim 6, claim is rejected on the same ground as for claim 1 because of similar scope. Furthermore, the PLL in FIG. 6 corresponds to the claimed control circuit.

Regarding claim 7, claim is rejected on the same ground as for claim 2 because of similar scope.

Regarding claim 8, claim is rejected on the same ground as for claim 3 because of similar scope.

Regarding claim 9, claim is rejected on the same ground as for claim 4 because of similar scope.

Regarding claim 10, claim is rejected on the same ground as for claim 5 because of similar scope.

Regarding claim 11, claim is rejected on the same ground as for claim 6 because of similar scope.

Regarding claim 12, claim is rejected on the same ground as for claim 7 because of similar scope.

Regarding claim 13, claim is rejected on the same ground as for claim 8 because of similar scope.

Regarding claim 14, claim is rejected on the same ground as for claim 9 because of similar scope.

Regarding claim 15, claim is rejected on the same ground as for claim 10 because of similar scope.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KCT

Khanh Cong Tran

KHANH C. TRAN
PRIMARY EXAMINER

1/6/2008
AU 2611